A Layout-Based Soft Error Rate Estimation and Mitigation in the Presence of Multiple Transient Faults in Combinational Logic

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***Abstract*—Cosmic radiation resulting in transient faults to the combinational logic of Integrated Circuits (ICs), constitutes a major reliability concern for space applications. In addition, continuous technology shrinking allows for the presence of Single-Event-Multiple-Transients (SEMTs), and renders modern chips more susceptible to soft errors. The study and evaluation of the impact of such errors on ICs functionality, as well as the pursuit of techniques to mitigate Soft Error Rate (SER), tend to become an essential part of the design process. This paper presents a Monte-Carlo-based SER estimation method, taking into account all masking mechanisms, which determines the vulnerable areas of a circuit based on layout information. Two layout-aware approaches are examined, the All-to-All and TMR-based, resulting in sufficient SER mitigation. The former, implies spacing among all components, while the latter converts the most sensitive components to a TMR structure, guaranteeing spacing between TMR triplet. The TMR-based approach leads to better SER mitigation compared to All-to-All, and produces better area and performance results.**

***Index Terms*—SER, Placement, SEMT, Masking Mechanisms, TMR, Radiation Hardening, Radiation Particles, Reliability**

I. Introduction

The rapid evolution in the field of VLSI technology over the past decades, has brought the emergence of Integrated Circuits (ICs) operating at high frequencies with low power requirements. Although modern chips become more efficient, transistor shrinking and supply voltage reduction, result in ICs becoming more susceptible to hazards, such as cosmic radiation [1]. Alpha particles emitted from radioactive impurities in package material, and high-energy particles, from cosmic radiation, may strike the IC silicon, producing Transient Faults (TFs). A soft error emerges when a generated TF is captured by a memory element, *i.e.* latch, flip-flop, or primary output and may result in circuit malfunction. The degree of circuit vulnerability to radiation-induced faults is represented by its Soft Error Rate (SER), and its estimation tends to be crucial to the chip design process. Thus, designers may apply various SER mitigation methods to create SER resistant chips.

Prior work focuses on the analysis of three masking mechanisms, *i.e.* logical, electrical and timing masking, to evaluate SER [2]. However, process technology shrinking has made modern chips more vulnerable, requiring analysis for Single-Event-Multiple-Transients (SEMTs). Reliability evaluation, particularly for combinational logic, becomes more crucial than for sequential elements for modern nanometer technologies [3]. Prior works may be divided into two categories, non layout-aware [4], [5] and layout-aware [3], [6]–[9]. The latter provide more accurate SER evaluation, as component placement influences hazard occurrence drastically. In particular, experimental results obtained by the methodology presented in [6], are quite reasonable, according to SPICE level verification, compared to the others. However, none of these works implement any SER mitigation technique, solely estimate SER. Recent studies have attempted to mitigate SER. In [10], a sensitivity-based gate sizing methodology is used, whereas in [11], authors propose a methodology for adding and removing redundant wires along with a gate resizing strategy to optimize SER robustness. However, even if they reduce SER, they do not take into consideration SEMTs which worsen the circuit reliability. Also, in [9] a placement-based radiation hardening technique is used, removing any whitespace between adjacent cells, which have common gates in their forward logic cones, thus increasing the probability of logical masking, and adding whitespace elsewhere. This technique may produce congestion issues, as many gates may share logic cones, and as a result the IC will be tightly packed. Moreover, state-of-the-art P&R tools are not SER-aware yet, as there is no efficient way to set SER as a placement constraint.

In this work, a detailed SER analysis for combinational logic, taking into account SEMTs and layout information is presented. Two different SER mitigation approaches are presented, which ensure SER reduction, rendering designs more resistant to external factors:

- All-to-All approach, which sets a spacing among all cells equal to the diameter of the particle's strike affected area, and
- Triple-Modular-Redundancy based (TMR-based) approach, which triples only the most critical cells, and

applies the same spacing among them.

The rest of the paper is organised as follows. Section II presents the methodology of sensitive region identification and the three masking effects; Section III highlights two important factors in SER estimation, *i.e.* the identification of the SEMTs and the handling of the reconvergent transient pulses; Section IV introduces the proposed placement approaches for SER reduction, the All-to-All and TMR-based; Section V elaborates the main SER estimation framework; Section VI provides experimental results of the proposed approaches on a set of ISCAS' 89 benchmarks and, finally, Section VII concludes this work.

II. Transient Faults Fundamentals

SER estimation requires the analysis of several parameters. Two critical ones include: (i) identifying cells sensitive regions, and (ii) taking into consideration three masking mechanisms, which determine when a glitch, generated at an affected cell output, will propagate through logic, and create a fault at a latching point, *i.e.* a flip-flop, latch or primary output.

A. Sensitive Regions

A TF can occur when a high-energy particle strikes on a transistor's depletion region. However, the emergence of a glitch at the output of an affected cell depends whether the particle strike affects the cell's sensitive area or not. Although the identification of these sensitive areas is a complex process, it is necessary for reliable SER estimation. Current pulse generation modeling and cell sensitivity characterisation require SPICE simulations. Current pulse generation is then performed, for both NMOS and PMOS transistors, and for all input combinations, each representing a particle hit. The generated pulse is observable as a transient voltage drop. Sensitive regions are then derived, as typically the cell's OFF transistors, when the pulse causes a change in output value [6].

B. Masking Mechanisms

Although a particle strike can cause a TF, the propagation of the latter can be stopped by three masking mechanisms, which essentially absorb it. The first mechanism, **logical masking**, occurs when a TF arrives at a cell's input, but another side input is a controlling value, thus preventing TF propagation, *e.g.* a controlling value of an AND gate is 0, for an OR gate is 1. Even if a TF is not logically masked, the intrinsic delay of the subsequent cells may attenuate its pulse width, to the point where it is eliminated before reaching latching points. This effect is called **electrical masking** and, for modeling pulse propagation, a linear function of the cell delay is used. The last mechanism that may prevent the capture of a TF from a memory element is **timing masking**. The latter depends on the pulse arrival time at a flip-flop and the latter's setup, hold window. Thus, a TF becomes masked if it reaches a flip-flop outside of this latching window.

III. Critical Factors for SER Estimation

SEMTs occur when a particle strike affects more than one adjacent cells causing multiple TFs. This phenomenon becomes more prevalent with the reduction of transistor sizes. Thus, the identification of SEMTs becomes critical for accurate SER estimation. Handling reconvergent transient pulses is also significant, as two or more pulses of the same TF may reach a fanout gate.

A. Identification of SEMTs

Given the physical layout of a circuit, a SEMT occurs, when a particle strike affects an area of the chip, producing glitches on adjacent cells [8]. The affected area is considered to be oval shaped, its diameter depending on the particle type, its Linear-Energy-Transfer (LET), and the strike angle [9]. With respect to modeling SEMTs, particle strikes may be considered to occur at random locations. The resultant oval shapes determine particle strikes' affected area, and thus affected transistors. If a sensitive transistor is within the strike range, a transient pulse occurs on the corresponding cell output. Identifying affected sensitive transistors, and subsequently affected cells, requires the exact cell positions, and their NMOS and PMOS diffusion positions, obtained by parsing the DEF and GDSII files. Inactive transistors within the oval area must also be checked [3]. Hence, by performing a rigorous physical layout analysis, an accurate SER estimation may be obtained. Some other approaches [4], [5] compute SER based only on the netlist, which is not as accurate, compared to the presented approach.

B. Reconvergent Transient Pulses

A significant issue regarding TF propagation, is the analysis and modeling of reconvergent pulses, as it has a great impact on the SER estimation [12]. Two or more pulses of the same TF may reach a fanout gate through different paths, hence their pulse width, direction, as well as arrival time may be different.

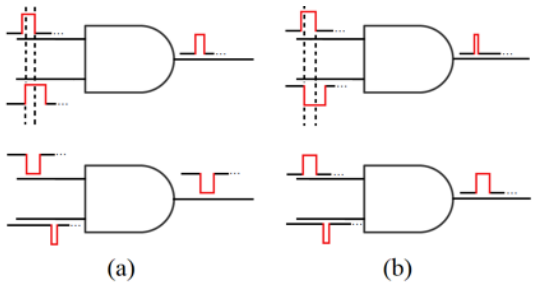


Fig. 1. Reconvergent pulses for AND gate for (a) Same direction. (b) Opposite direction.

To address this problem, and to form an appropriate output pulse, two factors are taken into consideration, *i.e.* the arrival times and the direction of different pulses, reconverging at a cell. When two reconvergent faults have the same direction and are overlapping, their output pulse is equal to the overlapping period, whereas when they are non-overlapping, only the

widest pulse emerges at the output, as shown in Fig. 1(a). On the other hand, for overlapping or non-overlapping faults in opposite directions, the resulting pulse at the output of the gate depends on its type and controlling value. For example, for an AND gate, the output pulse is computed using the logic 1 pulse, and by subtracting any overlapping portion, as the other input masks this interval, being a controlling value, *i.e.* logic 0. For non-overlapping pulses, the positive pulse is selected, as Fig. 1(b) shows. Reconvergent pulses for other gate types are computed in the same way. At this point, the resultant pulse is subjected to electrical masking, as described in Section II-B, to obtain its final signature.

IV. Placement Approaches for SER Reduction

Despite the masking mechanisms, cell physical positions may be used to reduce the impact of particles strikes further. Placement is an NP-Hard problem [13], focusing on placing design components at optimal positions in terms of PPA. One key disadvantage with industrial Place and Route (P&R) tools is that it is not feasible to use custom cost functions, *e.g.* SER. Furthermore, placement for radiation-hardening circuits has more constraints.

A high energy particle strike will likely affect more than one cell, in its incident spot area. There are two ways to achieve SER mitigation. One approach is to reduce the number of SEMTs, the other being to mask TF propagation. We investigate both approaches for reducing SER in this work. Our first approach introduces minimum spacing among all cells, equal to the diameter of the affected area (*i.e.* All-to-All approach), to reduce the number of SEMTs. Our second approach uses Triple-Modular-Redundancy (TMR) technique, to guarantee that the propagated signal of each TMR logic will not be affected. Fig. 2 shows implementation flows for: (i) original, non-radiation hardened circuit, (ii) All-to-All approach, and (iii) TMR-based approach.

A. All-to-All Approach

For the All-to-All approach, our main goal is to explore the impact of different spacing constraints on SER, timing and area. Increasing the spacing among all cells reduces the probability a SEMT to occur. All-to-All approach flow, as shown in Fig. 2 starts with a PPA optimised (IPO) placement solution, and then sets a specified spacing among all cells, spacing them apart from their initial positions [14]. Then, cells become fixed, to preserve their positions and the design is routed. This approach achieves that each particle strike affects only one gate, reducing the number of SEMTs occurred, and subsequently SER. However, large spacing among all gates increases both core area and wire delays. Thus, we also investigate the TMR approach, which applies a redundancy method to the circuit, to logically mask the occurred faults, instead of aiming to reduce the number of SEMTs.

B. TMR-Based Approach

Applying spacing among all of the design's cells is prohibitive, in terms of core area increase and delay penalties. An

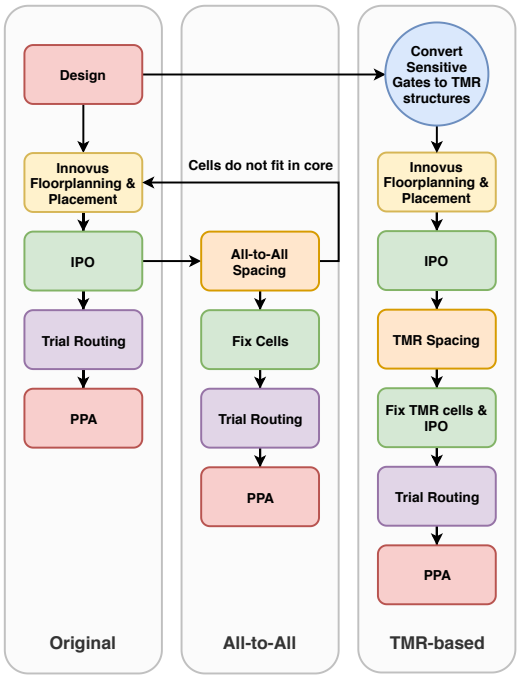
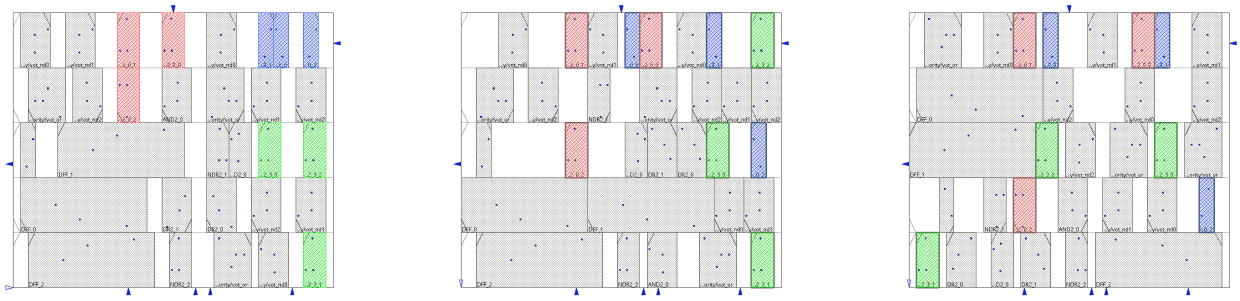


Fig. 2. Flow of proposed approaches

alternative approach to achieve a feasible solution is by adding redundancy to the circuit, thus preventing the propagation of any caused faults. In particular, this work utilises the Triple-Modular-Redundancy (TMR) technique. TMR is widely used in academia to guarantee that particle strikes do not affect the propagated TMR logic signals [15]. TMR logic consists of three identical gate instances, *i.e.* **TMR members**, and a voter, which propagates the majority result of the three gate outputs. The safest TMR approach triples all design gates (**Full-TMR**), to reduce the probability of a fault to propagate through the combinational logic. However, there are two drawbacks, (i) the circuit size is more than tripled, and (ii) modern state-of-the-art P&R tools cannot guarantee that a particle strike affects only one TMR member. Considering these drawbacks, it is preferable, in terms of PPA, to utilize the TMR technique only to a set of critical gates.

1) Critical Gates: A gate is regarded as a **critical gate**, when the probability of a generated TF, at its output, to propagate and reach a memory element is high. In such a case, the presence of the three masking effects that are able to mitigate a TF is vague. The process of gates' sensitivity characterisation focuses individually on each gate exposed on a definite number of particle strikes. Subsequently, the generated pulse is subjected to the three masking effects as it propagates through the circuit. To ensure that these factors hold a crucial role in obtaining reliable outcome regarding the gates sensitivity: (i) a sufficient number of simulations are performed, by applying numerous different primary input vectors, and (ii) fault pulses at gate output are simulated as wide enough, to potentially affect memory elements and the entire clock cycle is observed. Finally, the probability that all



(a) Without Spacing Constraint (b) 1.24um Spacing Constraint (c) 2.44um Spacing Constraint

Fig. 3. Placement layouts of ISCAS' 89 *s27* benchmark applying different spacing constraints

these faults are captured, by at least one sequential element, is obtained, by assigning a sensitivity value for each gate. Even though this process is time-consuming, due to the great number of simulations, and the resultant complexity for large-scale circuits, it provides an overview of the relative sensitivity among the gates of a given design. During the process for sensitivity identification we neglect SEMTs, as this process targets each gate separately. If SEMT analysis was considered, the sensitivity results would involve the adjacency of the gates which is not the case. On the contrary, for the selective hardening of the most critical gates only the sensitivity of the gate itself should be taken into account.

2) Critical-TMR approach: The proposing TMR-based approach, Fig. 2:

- Identifies the most sensitive, in terms of SER, gates,
- Utilises TMR technique only to the critical gates,
- Places TMR members with a distance among them, and
- Performs optimisations (IPO) to the non-TMR cells.

After critical gates extraction, TMR technique is applied solely to them, to reduce the design's SER with minimum area overhead. A new netlist is generated, and placement is performed in a state-of-the-art P&R tool, to obtain timing optimal gate positions. However, TMR members may be placed in close proximity, ignoring particle spacing constraints. Thus, a particle strike may affect two or even all the members of the TMR triplet, leading to TFs. To guarantee spacing constraints satisfaction, post-placement, the flow spaces out TMR members, using minimum displacement from their original positions [14]. Next, we fix the TMR members positions in the P&R tool, to ensure spacing violations cannot occur, and run placement optimisations (IPO), to improve PPA as much as possible. Finally, routing is performed. Fig. 3 shows layouts of a small design applying different spacing among the TMR members, highlighting each TMR triplet with different colours. In Fig. 3(a) placement, no spacing has been applied among each TMR structure members. Fig. 3(b) and 3(c) show layouts applying 1.24μm and 2.44μm spacing constraints, among TMR members respectively. Applying larger spacing will increase the wire length, and will also worsen timing. However, increasing spacing reduces the probability of a particle strike to affect more than one TMR member.

V. SER Evaluation Algorithm

A fundamental part of this work is also the detailed SER estimation, taking into consideration radiation-induced SEMTs in the circuit's combinational logic. The SER estimation method is based on topological analysis, by dividing the circuit layout to several smaller equal parts, *i.e.* grids. The number of grids may differ depending on circuit size, as for very small grids the extracted data may be misleading for SER evaluation. At random grid points, particle strikes, with different energies are simulated, generating multiple glitches. The generation and propagation of the SEMTs, as well as the masking mechanisms, are extensively discussed in [6]. Each generated fault is separately simulated. Thus, pulses, originated from a single particle strike, appearing at the output of affected cells, propagate throughout the circuit logic, along with their own logical, electrical and timing masking information. However, when the particle strike affects two or more TMR members, the generated faults are merged into one. Otherwise, the TMR voter will filter the individual faults, which is not the case.

The fault gate-level simulation uses the logical effort method for determining gate delay. Moreover, it models the masking effects to estimate the total latching probability per simulation, by checking the following cases:

1) The flip-flop input is affected by particle strike glitches, *i.e.* are not logically masked,
2) The glitch pulse width is wide enough to affect flip-flop input, and
3) The pulse arrives within the (setup, hold) timing windows

The total probability representing the circuit SER is computed, considering the latching probabilities, per simulation, for the different primary input vectors.

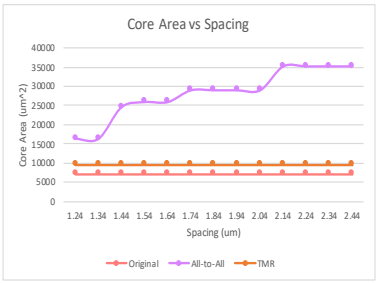
VI. Experimental Results

To compare the proposed radiation-hardening approaches, we used the 45nm NANGATE Library. Since this library does not contain any majority gate, we create one as a Verilog module.

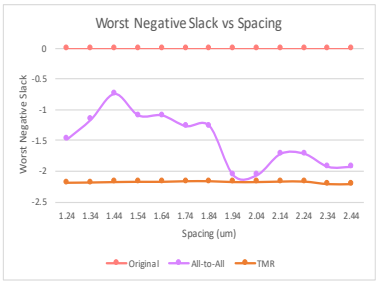
As mentioned, the applied minimum spacing among cells is equal to the area affected by the particle strike, which itself depends on several factors, such as particle's type, LET and

TABLE I
CORE AREA, SLACK AND AVERAGE SER FOR ISCAS' 89 BENCHMARKS

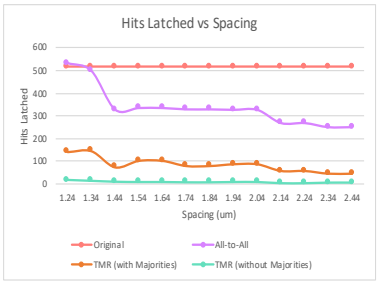
Design Name	Core Area (μm^2)			Worst Negative Slack (ns)			Average SER				SER Estimation Time (sec)			
	Original	All-to-All	TMR	Original	All-to-All	TMR	Original	All-to-All	TMR(Maj)	TMR(no Maj)	Original	All-to-All	TMR(Maj)	TMR(no Maj)
s27	31.920	181.944	57.190	0.541	0.469	0.321	0.2717	0.0638	0.0335	0.0096	2	1	3	2
s298	247.380	1572.858	522.690	0.046	-0.276	0.001	0.1184	0.0237	0.0123	0.0003	10	3	21	13
s400	335.160	2334.948	732.564	0.143	-0.209	-0.001	0.1016	0.0235	0.0094	0.0003	16	12	25	20
s1423	1303.400	11357.668	3288.558	-0.013	-0.488	-0.827	0.0450	0.0100	0.0043	0.0003	35	21	48	43
s9234	7050.596	29033.900	9550.464	0	-1.268	-2.162	0.0160	0.0061	0.0037	0.0001	305	215	903	879
s35932	30004.800	190839.040	66744.720	0	-5.170	-0.641	0.0275	0.0059	0.0054	0.0003	1500	1068	3610	1651
Average Ratio	1.00	6.04	2.08	1.00	-9.72	-4.63	1	0.25	0.14	0.01	1	0.6	1.98	1.46



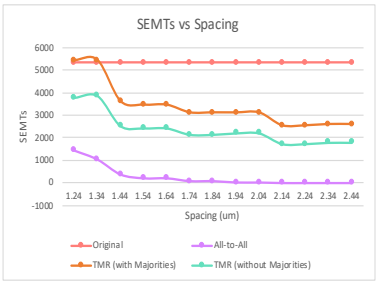
(a) Core Area vs Spacing



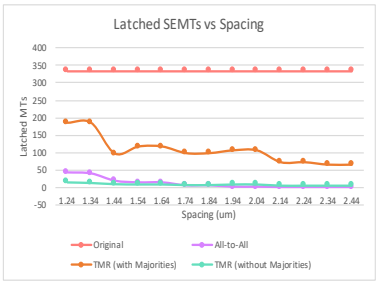
(b) Worst Negative Slack vs Spacing



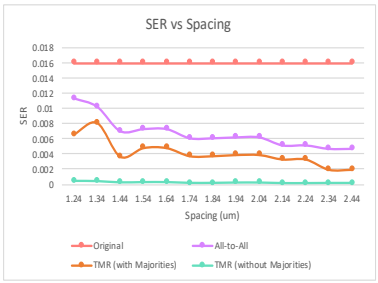
(c) Latched Hits (both SEMTs and SETs) vs Spacing



(d) SEMTs vs Spacing



(e) Latched SEMTs vs Spacing



(f) SER vs Spacing

Fig. 4. Area, Worst Negative Slack, Latched Hits, SEMTs, Latched SEMTs and SER behaviour of s9234 for different spacings

strike angle. To investigate the impact of our two approaches, as a function of applied spacing constraints, we tested 13 different spacings in the range [1.24, 2.44]µm. This range is based on [9], where the affected areas for particles with energies of 22, 47, 95 and 144 MeV are specified respectively. To generate our experimental results, we used 6 ISCAS'89 benchmarks, *i.e.* `s27`, `s298`, `s400`, `s1423`, `s9234` and `s35932`, and physical design was performed using Cadence®Innovus™.

Table I reports the Core Area, Worst Negative Slack (WNS), average SER and SER Calculation Execution Time, for the considered benchmarks. In this table, we present the results applying 1.84µm spacing across cells. This spacing is the mean of the examined spacing constraint range, so it is more representative than min (1.24µm) or max (2.44µm), as it balances between SER reduction and the PPA overhead. For the TMR-based approach, we converted the top 30% of the most critical gates to TMR modules, to restrict the impact on PPA.

It is important to note that for both All-to-All and TMR-based approaches, and each spacing value, we compute the SER by simulating the same number of particle strikes per unit area, *i.e.* particle flux. Thus, the results will be comparable between the two approaches, since the simulations are conducted under the same conditions, Fig. 5.

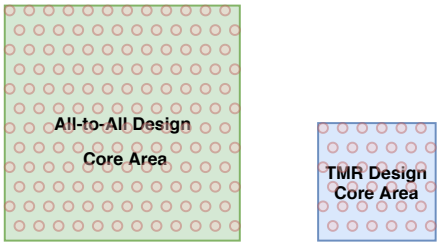


Fig. 5. The number of particle strikes per unit area is equivalent for both approaches

The All-to-All approach results, for all designs, in worse core area, compared to the TMR-based approach, while the latter leads to only slightly larger core area than the original design. On average, the All-to-All approach requires approximately 3 times larger core area, compared to TMR-based, to spread all the design's cells. With respect to WNS, behaviour is not monotonic. This can be caused by the IPO operations, that Innovus performs to improve PPA results. Considering SER results, the original design has worse SER, as no radiation-hardening technique had been applied. The effect of All-to-All and TMR-based approach is not equivalent, because All-to-All approach reduces the number of SEMTs compared to

TMR, which mainly logically masks the TFs caused in a TMR member. Comparing All-to-All and TMR-based approaches, the TMR-based approach leads to better SER results, which can be explained as follows.

- TMR-based approach reduces the number of SEMTs, although not as much as All-to-All does,
- Faults caused in the TMR logic are filtered by the voter compared to the All-to-All approach, where each fault can be propagated through the logic and be latched in a sequential element, and
- Given that the particle flux is the same for all designs, fewer particle strikes incident in TMR-based design compared to All-to-All one, since its core area is smaller than the others.

In the TMR-based approach, a common problem is a particle hit affecting the majority voter, making the masking mechanism ineffective. TMR technique can only filter faults occurring in one of the TMR members. In the case where a particle hits a majority gate, the error cannot be filtered. Various hardening-by-design techniques can be used to mitigate this problem, such as shielding the majority gates, sizing them up, or using delay elements with different delays per TMR member, rendering majority gates resistant to particle strike effects. We notice, that by ignoring majority gates in the SER calculation, the overall SER using the TMR-based approach is reduced further and it is almost equal to zero.

Overall, the average SER mitigation, contrasting All-to-All and TMR-based approaches, is approximately 75%, 86% and 99% respectively. In terms of SER calculation execution time, TMR-based approach takes twice as long to compute, as the number of gates is increased vastly after the TMR application. If majority gates are ignored, the execution time is improved, but not significantly compared to All-to-All approach and the Original. Furthermore, comparing the All-to-All approach with the original, non radiation hardening one, the former has slightly better execution time, as the observed SEMTs are less, because of the applied spacing. Therefore, the whole process, based on Monte-Carlo simulations, extends time-wise.

Fig. 4 presents the core area, WNS, latched hits, number of SEMTs, latched SEMTs and the average SER for the 13 different spacings applied to the `s9324` design. The original design presents the worst SER, but has best area and WNS. Both proposed approaches increase area and worsen WNS, but improve SER. It can be easily noticed that increasing the applied cells spacing, reduces SER, as the number of SEMTs is decreasing. Also, Fig. 4c presents the logical masking effect of the TMR-based approach, where the total number of TFs latched in a sequential element are significantly reduced compared to All-to-All approach. Thus, the TMR-based approach is a feasible solution to achieve SER mitigation, with good PPA results.

VII. Conclusions

We presented a detailed SER analysis for combinational logic, taking into account SEMTs and layout information. Two different SER mitigation approaches were presented and applied, which ensure SER reduction, the All-to-All approach, which sets a spacing equal to the diameter of the affected -by the particle strike area- among all cells, and the TMR-based approach, which triples only the most sensitive cells, and applies the same spacing between them. Experimental results indicate that TMR-based approach applied to most critical gates of the circuit achieves better SER mitigation compared to All-to-All approach, while having a small impact on the circuit PPA. A radiation-hardening-by-design technique applied to the majority voters renders SER mitigation even better.

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