# Placement-based SER Estimation in the Presence of Multiple Faults in Combinational Logic

Georgios Ioannis Paliaroutis†, Pelopidas Tsoumanis†, Nestor Evmorfopoulos†, George Dimitriou‡, Georgios I. Stamoulis‡

†Department of Electrical and Computer Engineering

‡Department of Electrical and Computer Engineering, and Department of Computer Science

University of Thessaly

37 Glavani St., Volos 38221, Greece

{gepaliar, petsouma, nestevmo, dimitriu, georges}@uth.gr

***Abstract*—Susceptibility of modern ICs to radiation-induced faults constitutes a matter of great concern in the recent years. Particularly, the transient faults and their impact on the combinational logic remain an intriguing issue, since the evaluation of their behavior is quite significant, especially for critical systems, for the development of error-resistant techniques in design process. For an accurate estimation of Soft Error Rate both single and multiple transient faults should be regarded since the appearance of the latter is more noticeable as technology downscales. The proposed tool, i.e. SER estimator, is based on Monte-Carlo simulations, in order to obtain an accurate result, and takes advantage of placement information to identify the vulnerable parts of a circuit. Finally, the verification shows a fairly good accuracy compared with SPICE.**

***Keywords—particle strike; masking mechanisms; multiple faults; placement; adjacent cells; SER***

## I. INTRODUCTION

Reliability in the area of VLSI design has always been a quite significant issue, let alone in recent years where the trend of the downscaling of the device feature sizes as well as the reduction in supply voltage result in a growing concern. In particular, the susceptibility of modern chips to *transient faults* (TFs) constitutes a continuous object of research.

Cosmic radiation and, specifically, high-energy particles that strike the silicon is considered to be the prevalent cause of such errors. Thus, their extensive study still remains a challenge since every chip that is exposed to cosmic rays is quite possible to be affected and present unexpected behavior with regard to its proper functionality. As soon as a particle strikes a transistor in a logic circuit, a charge disturbance inside the semiconductor is created, which results in a current/voltage pulse at the output of the corresponding logic gate [1, 2]. The generated fault is often referred to as a *single event transient* (SET). The SET that propagates through the circuit and is, finally, latched by a subsequent memory element is called a soft error. Although such errors do not cause permanent damage to the chip, the study of their influence on circuit's proper functionality is crucial especially for critical systems. The vulnerability of a circuit to soft errors is represented from *Soft Error Rate* (SER) and it is measured in *Failures In Time* (FIT).

However, as VLSI technology advances the modern ICs become even more dense and the distance between the cells decreases. Therefore, the probability that a single high-energy particle hit affects not only a single gate but a set of gates should be taken into account. In such a case a number of *multiple transient faults* (MTFs) are generated and propagate through the circuit. Thus, an analysis of the susceptibility of chips to radiation-induced errors could constitute a fundamental part of the chip design process aiming for reliable circuits.

In this work, an accurate and fast SER estimation is proposed considering MTFs and taking advantage of the layout information of the circuits. The analysis deals with particle strikes that occur on the combinational part of a circuit by modeling the three masking phenomena.

## II. RELATED WORK

The three masking phenomena are used from the majority of the approaches, that exist in the bibliography, in order to estimate SER [3, 4, 5, 6, 7, 8]. Single event upsets and single transient fault models are extensively studied in previous work [9, 10, 11]. Other approaches focus on probabilistic models and statistical methods in order to evaluate SER [12, 13, 14, 15]. Some of them do SPICE simulations to verify their results or to obtain parameters used in their methodologies [16, 17, 18, 19, 20]. The proposed methodology presented in [19] is based on binary decision diagrams (BDD) for the propagation of the error pulses and spice simulation to characterize the pulse generation. A logic cell and flip-flop characterization is conducted obtaining the parameters used in calculation of SER in [20].

Nevertheless, in the past few years, the downscaling of transistors' size and the reduction in supply voltage have made the modern circuits more vulnerable to high energy particle hits which, in turn, can affect multiple adjacent gates resulting in *Single Event Multiple Transients (SEMTs)* [21, 22, 23, 24]. In [25], the authors attempt to quantify the likelihood that a SET can cause multiple bit errors in combinational logic circuits consisting of gates

and flip-flops. The outcome of this work proves that the probability is quite significant, since it is very likely for a high energy particle hit to affect multiple cells of a circuit, and, therefore, multiple bit-flips should be taken into account in order to obtain a realistic fault model for soft errors. With respect to the multiple error sites, some methods consider that MTFs, at the logic level, are more likely to occur at the output of adjacent gates [26], while others present a layout-based SER estimation [22, 27, 28]. However, [27] merges the multiple faults and does not treat them individually, which may lead to inaccurate results. Furthermore, in [28], a grid-based method is used to pre-characterize the cells in order to obtain the induced SET pulse width at each grid point of the cell. The technique presented in [29] provides a fast and accurate probabilistic method, called Multiple Event Probability Propagation (MEPP). It considers that a MET occurs at the output of the physically adjacent gates which are identified at the gate-level by examining fan-outs and fan-ins.

This paper presents a detailed overview of a SER analysis for combinational logic of sequential circuits and focuses, mainly, on the modeling and handling of SEMTs originated from a single particle strike. Based on Monte-Carlo simulations and taking advantage of the layout information we obtain an accurate SER estimation.

The rest of the paper is organized as follows: Section III introduces the basics of fault generation and propagation; Section IV presents the proposed methodology and its algorithm as well as a detailed grid analysis; Section V shows the experimental results on the benchmark circuits and, finally, Section VI concludes this work.

## III. FAULT GENERATION AND PROPAGATION

Intensive research has been done so far in order to analyze and model the effect of transient faults in logic gates and circuits [9, 10]. In this section, we present in what way SETs affect a simple circuitry and how the masking phenomena prevent them from propagating through the circuits.

### *A. SET Pulse Modeling*

A practical way to observe and comprehend the behavior of an SET over a gate is to add a current pulse on a transistor node which, in turn, causes a voltage drop at the output of the gate. A parser which has been implemented in C parses a spice netlist and injects the current pulse at random internal transistors' nodes of each gate. A similar parser is also used in order to add transient faults in circuits and then simulate them using SPICE. Current pulses were inserted both to NMOS and PMOS nodes, since the progress of the rest simulation depends on the type of the transistor node on which the pulse has been injected. This process offers an overview of the effect of the transient faults on a circuit and shows how the initial duration and amplitude of a glitch attenuates, while passing through the ICs.

In the context of this work, the generated pulse can be described as a random variable with a particular probability density function (pdf) where the width of the output voltage pulse $w$ follows the uniform distribution. The widths of the pulses are discretized in N levels, as in [8], while the largest quantization value is equal to the period of the clock, since for pulse widths larger than that the memory elements will latch each glitch anyway.

### *B. Masking Mechanisms*

The tool that has been developed is based on the modeling and incorporation of the three natural masking effects into the whole process, in order to obtain an accurate SER of digital ICs. As already mentioned, SETs that may occur on any gates' inputs or output of a circuit may propagate through the subsequent cells and lead to soft errors if some of them are latched by memory elements (flip-flops). However, the three mechanisms that provide to circuits a kind of natural resistance to faults and determine whether transient faults will propagate to become a soft error, or not, are logical, electrical and timing masking.

***Logical masking*** occurs when the propagation of a transient fault through a circuit until the memory elements' input is prevented, due to a subsequent gate whose output is completely controlled by one or more inputs. For instance, if at least one of the inputs of an OR gate has logic value 1, its output will always be logic 1 regardless of the glitch that arrives on another input of the gate. In a similar way, an AND gate's output will always be logic 0 if at least one of its inputs has logic value 0. ***Electrical masking*** is the second factor that prevents an error from reaching the flip-flops and, thus, protects the circuit from an unexpected behavior. A SET is electrically masked when the pulse resulting from a particle hit is attenuated due to the electrical properties of the gates on its propagation path so that the resulting pulse is of insufficient magnitude to be reliably latched. Last but not least, the third factor which contributes to the elimination of such disturbances in the circuits is ***timing masking*** and occurs when a transient fault arrives at the input of a flip-flop outside of the latching window where the memory element capture the input value.

## IV. SER ANALYSIS FRAMEWORK

In this section, a layout-based SER estimation in the presence of MTFs in combinational logic is presented. Afterwards, we describe how the masking mechanisms are incorporated into the proposed tool, elaborating the structure of the respective algorithm, along with a grid analysis approach in order to provide a preview of circuits' vulnerability to such type of errors.

### *A. Placement-aware Analysis of SEMTs*

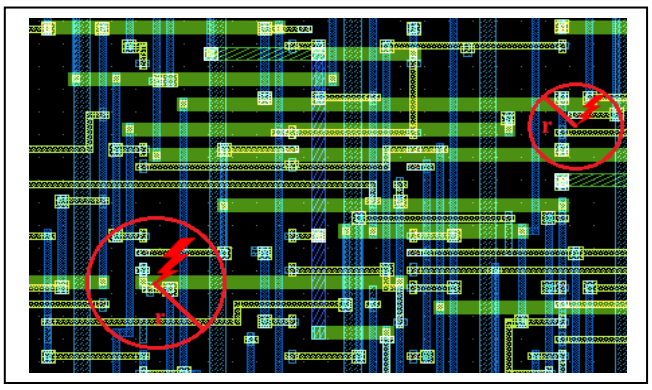
SEMTs occur when a particle hit does not affect only a single point over the chip but an area which should be defined properly for an accurate particle strike simulation. This area is mostly a function of particle energy and the higher the amount of energy is, the wider the area of the circuit that is affected by the strike. The surface affected by a particle hit is depicted with oval shapes, according to the average affected area for each particle's energy, as shown in Table I [22].

TABLE I. AVERAGE AFFECTED AREA

| Particle Energy (Mev) | Average Affected Area ($\mu m^2$) |
|---|---|
| 22 | 1.178 |
| 47 | 1.902 |
| 95 | 2.903 |
| 144 | 4.613 |

With regard to the implementation of this novel SEMTs approach, particle hits are injected on random points into the die area of each circuit. The corresponding oval shapes indicate which gates are affected by each particle strike. In order to identify the gates that belong to error sites, the radius of the oval shape has been used, which corresponds to the range that a particle hit affects, as shown in "Fig. 1". If a gate is located within the range of the strike, a SET is created on the respective gate's output. Furthermore, "Fig. 1" shows the result, with respect to the affected area, of two particle strikes with different energies.

Fig. 1. Particle strikes of different energy



A significant step for the SEMT analysis is the identification of the physically adjacent cells of each circuit and for this purpose the *DEF (Design Exchange Format)* files - for the corresponding ISCAS' 89 benchmark circuits - have been utilized. These files which are generated by place and route tools are used to represent the position and placement direction of each logic cell in the layout. Therefore, our methodology is based on gates' placement locations of each circuit and the aforementioned methodology for the masking phenomena in order to estimate SER. Particularly, instead of checking the fan-ins and fan-outs of each gate to find the adjacent sites, the topological adjacency of the circuit's gates is analyzed by keeping the topological information that deals with the die size and the coordination of the gates. However, there are approaches which rely only on logic-level netlist, neglecting cells' adjacency but instead, considering a gate and its fan-ins, a gate and its fan-outs, fan-ins of a gate and fan-outs of a gate as adjacent nodes for multiple transients' error sites [26, 29]. In this context, when a particle strikes a random area of a circuit and affects a gate, its fan-out may lead to a gate which does not belong to the same error sites, according to the topological information drawn from the DEF files. Thus, considering only logic-level netlists during the analysis leads to inaccurate estimation of SER, since, with this method, a restricted number of cells are physically adjacent.

### B. *Proposed Algorithm*

Due to the downscaling of transistors' size and reduction in supply voltage, circuits have become more vulnerable to particle hits and the presence of SEMTs is more intense. Consequently, for the estimation of SER both SETs and SEMTs should be considered [21, 22, 23]. The base of the proposed methodology for the extraction of SER is Monte-Carlo simulation. In order to obtain accurate results a sufficient number of Monte-Carlo simulations for each circuit have been made. Therefore, the execution of *10,000* simulations with different input vector each time seems to be adequate, since when this number increases there is not much deviation in the results. Even though this method is time consuming we prefer it from other probabilistic methods since provides more secure outcome. For this reason, several acceleration techniques, applied on our tool, improved the simulation time especially for the large-scale benchmark circuits. A couple of these methods are described in the Section V.

The tool that has been implemented is based on a simple zero-delay gate-level simulator. Particularly, the method of logical effort is utilized for finding the delay of each gate, since it is supposed to be a straightforward and useful delay model. The logical, electrical and timing masking mechanisms are the main parts of this work and their modeling is a necessary process for the SER evaluation. In order to analyze extensively SEMTs arisen in *errors-gen* function according to the following algorithm, as well as their masking effects, we use tables for each node of the circuit to examine each error separately, and determine those that will be captured by the memory elements. Particularly, two tables are used for logical and timing masking, which are *temp_error_state* and *error_time* respectively, as shown in "Fig. 2". Their size, which changes dynamically, depends on the number of transient faults originated from a single particle strike.

Fig. 2. SER calculation

```
Algorithm 1 Compute SER
  def : Design Exchange format file
  procedure FILE(def)
      create-circuit(def);
      find-delay(def);
      logical-masking(def);
      for each grid in def do
          errors=errors-gen(grid);
          for 10000 simulations do
              for each node in def do
                  for i=0 to errors do
                      compute temp-error-state[i]
                  end for
                  electrical-masking(node);
                  timing-masking(node); //compute error-time[i]
              end for
          end for
          total-latching-prob();
      end for
      overall-SER();
  end procedure
```

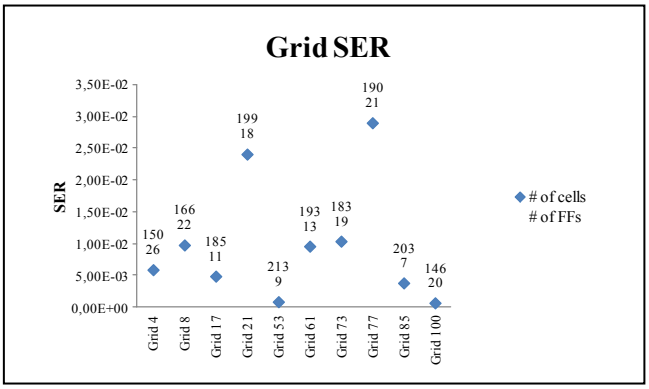
As regards the modeling of logical masking for SEMTs the corresponding table shows the logic state of each node and how it is affected by each fault. In other words, it is examined which faults propagate through the circuit to the inputs of the flip-flops and which are logically masked. For the timing masking effect it is necessary to compute the overall time (*error_time*) for each fault, that is, the time it takes to reach the flip-flop from the moment of the SEMTs incident. A glitch is captured by a flip-flop only if it arrives on the data input during the latching window of the flip-flop. The third factor is electrical masking and is modeled along with the aforementioned mechanisms. The glitches caused by a particle hit have initially the same width and the main factor which affects their value are the gates' delay. Masking effects are used to estimate the total latching probability of each circuit in *total_latching_prob* function. In comparison with other techniques, we do not determine latching probability for each flip-flop, but only one for each simulation, comparing initially the input logic state of each flip-flop with the pointer estimated for the logical masking and then all together. At the end, in *overall_SER* function the overall SER of the procedure is estimated taking into account the latching probabilities of each simulation.

### C. Grid Analysis

The purpose of a well-designed and accurate SER estimation tool, like the one that is proposed, is to provide to VLSI designers an overview of the vulnerability of a circuit so as, by applying the suitable restrictions and making tradeoffs between power, performance and reliability, they will be able to construct error-resistant chips.

In this context, the layout of each circuit has been equally divided into a hundred smaller parts, called so on grids, and are considered as small sub-circuits. Particularly, a number of particle hits are injected on each grid causing a different number of errors since each sub-circuit includes its own set of logic cells placed in this area. Afterwards, the aforementioned methodology is applied for each grid in order to obtain the overall SER of the circuits. This process facilitates the identification of susceptible sites as well as the extraction of reliable outcomes by exciting the entire circuit. "Fig. 3" shows the SER of some grids of S35932 benchmark circuit taking into account the number of gates and flip-flops.

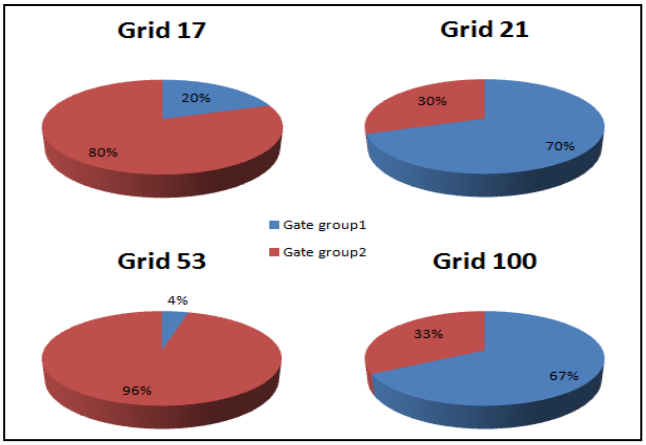
Fig. 3. GRIDS' SER of S35932




We conclude from this graph that the grids which contain a large number of gates and flip-flops are more probable to have a greater overall number of errors occurred from a particular number of particle hits. However, something that should be underlined is that the existence of many faults in some blocks does not mean that the respective SER is greater than others' with less. Particularly, the estimation of SER depends on the type of gates that are located on each grid and how the masking effects influence this process. For example, although sub-circuits 53 and 100, as shown in "Fig. 3", have several gates and flip-flops, their SER is approximately zero. Thus, it could be deduced that these factors may affect more drastically these grids or, maybe, the energy of the particle strikes on these parts of the circuit was not intense enough to cause many errors.

Furthermore, we infer from these results that sensitive grids should be regarded those that are close to flip-flops, since generating pulses are more possible to reach at the memory elements. We consider as *Gate group1* the number of the gates of each grid that lead to flip-flops that belong to the same grid with them. Nevertheless, some gates, which belong in *Gate group2*, may lead to flip-flops which are located to other grids. This could explain the fact that different sub-circuits, which have similar number of gates and FFs, have a significant difference in SER. For instance, in "Fig. 3" and "Fig. 4", the SER and the percentage of gates of group1 for grid 21 are both greater compared to the respective for grid 17. For the grid 100, as mentioned previously, the calculation of SER may be affected by the masking factors, since, as shown in "Fig. 4", the fact that the majority of its gates lead to flip-flops of the same grid does not explain the almost zero value of SER. On the other hand, as regards grid 53, the principal cause of such a low SER seems to be the connection between its gates and the memory elements, since only 9 gates drive flip-flops of the same grid.

Fig. 4. Gates' connectivity with FFs of S35932




The behavior of such hits over a circuit could be examined further by dividing each grid into smaller sub-grids in order to focus on a smaller area. A large number of sub-grids means a more detailed analysis since we can determine which masking factor dominates over the other ones. Afterwards, it is counted how many hits occur on

each sub-grid, obtaining, in this way, the density of the hits on each grid and the percentage of errors that become logically, electrically and timingly masked.

By computing the density and taking into consideration the effect of masking phenomena on grid's SER, as well as topological information of each sub-grid, we could be able to extract conclusions about the vulnerability of chips to particle hits and contrive ways to design error-resistant chips with enhanced placement techniques.

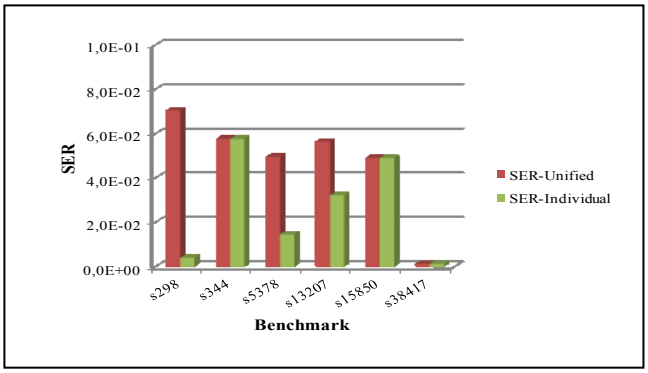
## V. RESULTS

In this section, we will present the results of the experiments that the implemented tool made with the help of various tables. For this purpose, as already mentioned, *ISCAS'85 and ISCAS'89* benchmark circuits have been used and this tool was run on an Intel Core i3-4005U @1.7GHz machine with 4 GB RAM.

For a faster simulation several techniques have been used. One of them is to hold the logic state of each node on an *unsigned int* variable where each position of the 32-bit number corresponds to one separate simulation. In this way, we take advantage of all possible combinations of primary inputs. Therefore, at the end of a single iteration, 32 different primary inputs have been used and, thus, 32 different simulations have been completed. A crucial point for the simulation is that the generated faults from an individual hit propagate through the circuit as individual faults, with their own timing and width properties, and they are not merged on a single fault which provides an accurate estimation of SER.

"Fig. 5" shows the overall SER of some benchmark circuits. In the first case, the produced errors from a particle strike are treated in a unified way while they propagate through the circuit. However, in the second one, the propagation of the errors is handled individually, which means that each error has its own width and arrival time at the flip-flops. This process provides, in most cases, even more secure results, since it simulates precisely the modeling and propagation of the multiple faults.

Fig. 5. SER of unified and individual errors



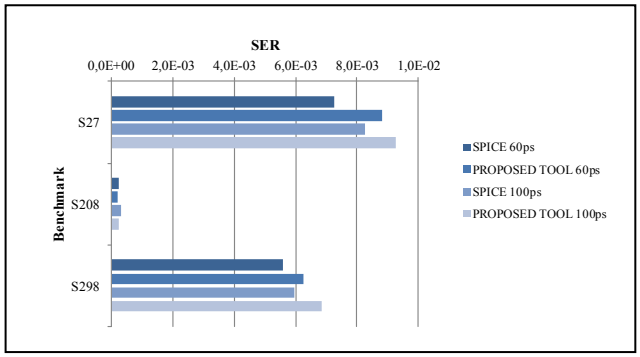

The following table presents the evaluation of SER obtained from the proposed tool for some benchmark circuits, as well as the corresponding execution time.

TABLE II. SER AND EXECUTION TIME OF BENCHMARK CIRCUITS

| Benchmark | # of nodes | # of gates | # of DFFs | SER | Exec. time |
|---|---|---|---|---|---|
| S400 | 192 | 188 | 21 | 0.011695 | 37 sec. |
| S1423 | 750 | 733 | 74 | 0.015191 | ~ 3 min. |
| S9234 | 5870 | 5834 | 211 | 0.016189 | ~ 28 min. |
| S15850 | 10425 | 10348 | 534 | 0.028721 | ~ 51 min. |
| S35932 | 17837 | 17802 | 1728 | 0.003910 | ~ 2.5 h. |

We use SPICE simulator in order to verify the obtained results from our implementation for the sequential circuits S27, S208 and S298 ("Fig. 6"). Even though SPICE is a reliable tool, it was utilized only for these three benchmarks and for SET analysis because this process is time consuming especially for larger circuits. For this reason, for each circuit, only one hundred simulations are carried out injecting a current pulse to a random node of each SPICE netlist and on different time moments. Therefore, it should be underlined that our tool can be regarded more accurate in comparison with SPICE simulations since a number of *10,000* simulations provide a reliable estimation of SER.

Fig. 6. SER verification




These benchmarks are simulated for different input vectors which respond to separate test patterns. A factor that affects, to an important degree, the estimation of SER is the initial duration of a glitch which is assumed to be *60ps* and *100ps*. According to "Fig. 6" increasing the width of the glitch SER becomes greater for both Spice's and our tool's simulations. This fact is absolutely reasonable since transient faults produced from particle strikes with higher energy are more likely to be latched by memory elements. The low SER value for the S208 benchmark could be explained from the complexity of its layout compared to the respective layouts of the other two benchmarks. Furthermore, the operating voltage at *1.25V* has made modern technology circuits more sensitive in contrast to older ones, since it is easier for a transient pulse injected on a node to exceed half of the *Vdd* value and, eventually, turn into a soft error. Another factor which affects the SER is the operating frequency of the circuit. In our case, we consider that the period of the clock is *250ps*. Finally, increasing the operating frequency, the probability that a transient fault will be latched will be enhanced, since the number of clock rising edges are increased [17].

## VI. CONCLUSION

In this work, a Monte-Carlo-based approach for accurate estimation of the vulnerability of ICs to radiation-induced faults is proposed, taking into consideration MTFs. In this direction, the placement details of each circuit are utilized for the identification of the multiple transients. Furthermore, a topological analysis provides to VLSI designers information about the sensitivity of particular parts of a chip. This could facilitate the process of error-resistant circuits development. Finally, *ISCAS'89* benchmarks have been used in order to demonstrate the results.

## REFERENCES


[1] Seifert, N., Slankard, P., Kirsch, M., Narasimham, B., Zia, V., Brookreson, C., Vo, A., Mitra, S., Gill, B., Maiz, J., "Radiation-Induced Soft Error Rates of Advanced CMOS Bulk Devices," Reliability Physics Symposium Proceedings, 2006. 44th Annual., IEEE International , vol., no., pp.217,225, 26-30 March 2006.

[2] Messenger, G.C., "Collection of Charge on Junction Nodes from Ion Tracks," Nuclear Science, IEEE Transactions on , vol.29, no.6, pp.2024,2031, Dec. 1982.

[3] Cha, H., Rudnick, E.M., Patel, J.H., Iyer, R.K., Choi, G.S., "A gate-level simulation environment for alpha-particle-induced transient faults," Computers, IEEE Transactions on , vol.45, no.11, pp.1248,1256, Nov 1996.

[4] Dhillon, Y.S., Diril, A.U., Chatterjee, A., "Soft-error tolerance analysis and optimization of nanometer circuits," Design, Automation and Test in Europe, 2005. Proceedings , vol., no., pp.288,293 Vol. 1, 7-11 March 2005.

[5] Zhao, C., Bai, X., Dey, S., "A scalable soft spot analysis methodology for compound noise effects in nano-meter circuits," Design Automation Conference, 2004. Proceedings. 41st , vol., no., pp.894,899, 7-11 July 2004.

[6] Murley, P.C.; Srinivasan, G.R., "Soft-error Monte Carlo modeling program, SEMM," *IBM Journal of Research and Development* , vol.40, no.1, pp.109,118, Jan. 1996.

[7] Zhang, M., Shanbhag, N.R., "A soft error rate analysis (SERA) methodology," Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conference on , vol., no., pp.111,118, 7-11 Nov. 2004.

[8] Bountas, D., Stamoulis, G.I., "CARROT – A Tool for Fast and Accurate Soft Error Rate Estimation",Embedded Computer Systems: Architectures, Modeling, and Simulation Lecture Notes in Computer Science, vol. 4017, pp 331-338, 2006.

[9] Rao, R.R., Chopra, K., Blaauw, D.T., Sylvester, D.M., "Computing the Soft Error Rate of a Combinational Logic Circuit Using Parameterized Descriptors," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , vol.26, no.3, pp.468,479, March 2007.

[10] AlQuraishi, E., Al-Roomi, M., Almukhaizim, S., "Analysis of the soft error susceptibility and failure rate in logic circuits." IEEE Int. Arab J. Inf. Technol. 8.4 (2011): 388-396.

[11] R.R. Rao , K. Chopra , D. Blaauw , D. Sylvester, " An Efficient Static Algorithm for Computing the Soft Error Rates of Combinational Circuits." IEEE Design, Automation and Test in Europe, 2006. DATE '06. Proceedings.

[12] J. S. Kim, C. Nicopoulos, N. Vijaykrishnan, Y. Xie, E. Lattanzi,"A Probabilistic Model for Soft-Error Rate Estimation in Combinational Logic ." IEEE 1st International Workshop on PROBABILISTIC ANALYSIS TECHNIQUES FOR REAL TIME AND EMBEDDED SYSTEMS (PARTES2004) (September 2004).

[13] Fan Wang , Vishwani D. Agrawal,"Soft error rate determination for nanoscale sequential logic .", IEEE Quality Electronic Design (ISQED), 2010 11th International Symposium on.

[14] Yu-Hsin Kuo , Huan-Kai Peng , Charles H.-P. Wen," Accurate statistical soft error rate (SSER) analysis using a quasi-Monte Carlo framework with quality cell models .", IEEE Quality Electronic Design (ISQED), 2010 11th International Symposium on.

[15] Mohammad Hosseinabady , Pejman Lotfi-Kamran , Jimson Mathew, Saraju Mohanty , Dhiraj Pradhan" Single-Event Transient Analysis in High Speed Circuits ." IEEE Electronic System Design (ISED), 2011 International Symposium on, 19-21 Dec. 2011.

[16] Miskov-Zivanov, N., Marculescu, D., "Soft Error Rate Analysis for Sequential Circuits," Design, Automation & Test in Europe Conference & Exhibition, 2007. DATE '07 , vol., no., pp.1,6, 16-20 April 2007.

[17] Miskov-Zivanov, N., Marculescu, D., "MARS-C: modeling and reduction of soft errors in combinational circuits," Design Automation Conference, 2006 43rd ACM/IEEE , vol., no., pp.767,772.

[18] Gill, B.S., Papachristou, C., Wolff, F.G., "Soft Delay Error Analysis in Logic Circuits", Design, Automation and Test in Europe, 2006. DATE '06. Proceedings , vol.1, no., pp.1,6, 6-10 March 2006.

[19] Bin Zhang , Wei-Shen Wang , M. Orshansky" FASER: fast analysis of soft error susceptibility for cell-based designs", Published in: Quality Electronic Design, 2006. ISQED '06. 7th International Symposium on, 27-29 March 2006.

[20] R. Rajaraman , J.S. Kim , N. Vijaykrishnan , Y. Xie ; M.J. Irwin, " SEAT-LA: a soft error analysis tool for combinational logic", Published in: VLSI Design, 2006. Held jointly with 5th International Conference on Embedded Systems and Design., 19th International Conference on, 30 January 2006.

[21] Kiddie, B.T., Robinson, W.H., Limbrick, D.B., "Single-Event Multiple-Transients (SEMT): Circuit Characterization and Analysis." IEEE Workshop Silicon Errors in Logic—System Effects (SELSE), Palo Alto, CA, USA. 2013.

[22] Ebrahimi, M., Asadi, H., Tahoori, M.B., "A layout-based approach for Multiple Event Transient analysis," Design Automation Conference (DAC), 2013 50th ACM / EDAC / IEEE , vol., no., pp.1,6, May 29 2013-June 7 2013.

[23] Miskov-Zivanov, N., Marculescu, D., "A systematic approach to modeling and analysis of transient faults in logic circuits," Quality of Electronic Design, 2009. ISQED 2009. Quality Electronic Design , vol., no., pp.408,413, 16-18 March 2009.

[24] D. Rossi , M. Omana , F. Toma , C. Metra, " Multiple transient faults in logic: an issue for next generation ICs?", Published in: Defect and Fault Tolerance in VLSI Systems, 2005. DFT 2005. 20th IEEE International Symposium on, 3-5 Oct. 2005.

[25] Nanditha, P.R., Shahbaz, S., Madhav, P.D., "On the likelihood of multiple bit upsets in logic circuits." arXiv preprint arXiv:1401.1003, 2014.

[26] Miskov-Zivanov N., Marculescu, D., "Multiple Transient Faults in Combinational and Sequential Circuits: A Systematic Approach," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , vol.29, no.10, pp.1614,1627, Oct. 2010.

[27] Paliaroutis, G. I., Tsoumanis, P., Dimitriou, G., & Stamoulis, G. I. (2016, September). SER Analysis of Multiple Transient Faults in Combinational Logic. In Proceedings of the SouthEast European Design Automation, Computer Engineering, Computer Networks and Social Media Conference (pp. 36-41). ACM.

[28] Yankang Du , Shuming Chen, " A Novel Layout-Based Single Event Transient Injection Approach to Evaluate the Soft Error Rate of Large Combinational Circuits in Complimentary Metal-Oxide-Semiconductor Bulk Technology", Published in**:** IEEE Transactions on Reliability, Volume: 65,pp.248-255, March 2016.

[29] Fazeli, M., Ahmadian, S.N., Miremadi, S.G., Asadi, H., Tahoori, M.B., "Soft error rate estimation of digital circuits in the presence of Multiple Event Transients (METs)," in Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011 , vol., no., pp.1-6, 14-18 March 2011.