A Placement-aware Soft Error Rate Estimation of Combinational Circuits for Multiple Transient Faults in CMOS Technology

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***Abstract*—A considerable disadvantage that comes with the downscaling of the CMOS technology is the ever-increasing susceptibility of Integrated Circuits (ICs) to soft errors. Therefore, the study of the radiation-induced transient faults in combinational logic has become one of the most challenging issues as the absence of appropriate error-protection mechanisms may lead to system malfunctions. This paper presents an efficient and accurate layout-based Soft Error Rate (SER) estimation analysis for ICs in the presence of both single and multiple transient faults, since the latter are more prevalent as technology downscales. The proposed tool, i.e. SER estimator, is based on Monte-Carlo simulations taking into account a detailed grid analysis of the circuit layout for the identification of the vulnerable areas of a circuit and, in addition, temperature as one of the factors that affect the generated pulse width. The widening of the fault pulses due to elevated temperature is reflected in increased SER according to our results. Finally, the comparison between the simulation results for some of the *ISCAS'89* benchmark circuits obtained from the proposed framework and the respective ones obtained from SPICE indicates a fairly good correlation.**

I. INTRODUCTION

The reliability of VLSI ICs has always been a matter of great concern, especially in recent years, due to the technology downscaling as well as the reduction in supply voltage and node capacitance. In particular, *transient faults* (TFs) induced by neutron strikes constitute a serious threat for the susceptibility of modern chips [1], [2]. Cosmic radiation and, specifically, high-energy particles that strike the silicon is considered to be the prevalent cause of such errors. Although they do not cause permanent damage, their extensive study is crucial and still remains a challenge especially for critical systems exposed to cosmic rays. When a particle strikes a transistor, a charge disturbance inside the semiconductor is created, which results in a voltage pulse at the output of the corresponding cell [3], [4]. The generated fault is often referred to as a *single event transient* (SET). The SET that propagates through the circuit and is, finally latched by a memory element is called a soft error. The vulnerability of a circuit to soft errors is represented from *Soft Error Rate* (SER) and is measured in *Failures In Time* (FIT).

As VLSI technology downscales, resulting in decreasing distance between the cells, the probability that a high-energy particle will affect a set of gates should be accounted for. In such a case *multiple transient faults* (MTFs) are generated and propagate through the circuit. Thus, an analysis of the susceptibility of chips to radiation-induced TFs could constitute a crucial part of a reliable chip design process.

The characterization and modeling of soft errors in combinational logic taking into account the three masking phenomena constitute the main object of other published work [5]-[7]. Single event upsets and single transient fault models are extensively studied in [8] and [9]. Some works focus on probabilistic models and statistical methods for the estimation of SER [10]-[13], while others use a SPICE tool to verify their results or to obtain parameters used in their methodologies [14]-[17]. The methodology presented in [16] is based on binary decision diagrams (BDD) for the propagation of the error pulses, and SPICE simulation to characterize the pulse generation.

As technology downscales, modern circuits become more susceptible to high-energy particle strikes and, thus, it is more likely that multiple adjacent cells will be affected resulting in *Single Event Multiple Transients (SEMTs)* [18]-[23]. Heavy-ion test results are presented in [20] for the detailed characterization of SEMTs. The authors in [24]-[26] introduce the determination of sensitive zones for the estimation of SER. In [27] and [28] a SEMT is considered to occur at the output of physically adjacent gates which are identified by examining the netlist. However, neglecting the layout-level adjacency of the cells and utilizing only logic-level netlists for the determination of circuits' error sites may lead to inaccurate results. On the other hand, layout-based approaches provide a more realistic SER es-

timation analysis [25], [26], [29]-[31]. Furthermore, in [30], a grid-based method is used to pre-characterize the cells in order to obtain the induced SET pulse width at each grid point of the cell.

This paper presents a detailed overview of SER analysis for combinational logic of sequential circuits and focuses, mainly, on the modeling and handling of SEMTs originating from a single particle strike. Based on Monte-Carlo simulations and taking advantage of the layout information we obtain an accurate SER estimation. The rest of the paper is organized as follows: Section II introduces the basics of fault generation and propagation; Section III presents the proposed methodology and its algorithm as well as a detailed grid analysis; Section IV shows the experimental results on the benchmark circuits and, finally, Section V concludes this work.

II. TRANSIENT FAULT ANALYSIS

Intensive research has been performed in order to analyze and model the effect of transient faults in logic gates and circuits [5], [11]. In this section, we present in what way SETs affect a simple circuitry, which are the sensitive zones of a cell, and how the masking phenomena prevent them from propagating through the circuits.

A. SET Pulse Characterization

As mentioned, TFs are caused by a high-energy particle strike on a transistor's depletion region (an off transistor of a gate). Fortunately, the generated glitch does not damage the transistor, though it may momentarily flip the state of the output node. In order to characterize gate sensitivity, it is necessary to perform simulations for each cell [8], [16].

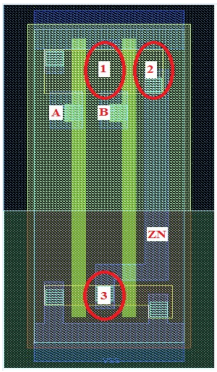
A practical way to observe and comprehend the impact of a SET on a gate is to add a current pulse to the transistor node, which, in turn, causes a voltage drop at the output of the gate. Thus, a SET is modeled and we are able to evaluate the robustness of transistors. The impact of such errors on each gate can be determined by the input values since both transistors (NMOS and PMOS) hold an essential role in the fault analysis. It should be emphasized that error events are simulated differently on each transistor type. In particular, a fault on a NMOS is simulated with a current pulse injected into the drain and extracted from the body of the transistor, while on a PMOS the current pulse enters the body and exits from the drain.

This process offers an overview of the effect of the TFs on a circuit and shows how the initial duration of a glitch attenuates, while passing through the ICs, considering various capacitive loads on the output nodes of affected gates. Simulations show that the generated faults tend to be filtered as capacitive load increases [4], [31].

B. Sensitive Zones

The method of transient fault injection into SPICE netlists has been presented in the previous subsection. In order to incorporate an accurate fault injection model into the proposed framework, it is necessary to parse the GDSII file of each cell for the identification of the transistor's diffusion area. The definition of these regions forms a significant step, since, as a result of technology downscaling, the circuits become denser and, thus, a single particle strike may affect more cells as will be discussed.

The physical structure of an inverter is quite simple and there are only two sensitive regions, the NMOS and PMOS drain. However, the identification of the susceptible zones for the other cells depends on their inputs. Therefore, we are able to obtain these zones since a particle strike affects the operation of a cell only if it occurs on the inactive transistors [24]-[26].



A	B	ZN	Sensitive Zones
0	0	1	Region3
1	0	0	Region1
0	1	0	Region2
1	1	0	Region1&Region2

Fig. 1. Sensitive zones of a NOR gate

As an example, Fig. 1 demonstrates the physical layout of a NOR gate with two inputs as well as the three sensitive regions. It should be noted that the parts of the diffusions connected to the supply line and the ground are not affected from the collection of the additional charge and, thus, are not considered as vulnerable zones. The table in Fig. 1 shows the sensitive regions for each input combination. In the same way, all the cells are characterized in order to determine the sensitivity of each region to particle strikes [26].

C. Masking Mechanisms

The tool is based on the modeling and incorporation of the three masking effects, in order to obtain an accurate SER of digital ICs. As already mentioned, SETs that may occur on any gate input or output may propagate through the subsequent cells and lead to soft errors if it is latched by memory elements. However, this may be prevented by logical, electrical and timing masking [10].

Logical masking occurs when the propagation of a TF through a circuit until the memory element input is prevented due to a subsequent gate whose output is completely controlled by one or more inputs. For instance, if at least one of the inputs of an OR gate has logic value 1, its output will always be logic 1 regardless of the glitch that arrives on another input of the gate. In a similar way, an AND gate's output will always be logic 0 if at least one of its inputs has logic value 0. ***Electrical masking*** is another factor that prevents an error from reaching the *flip-flops* (FFs) and, thus, protects the circuit from an unexpected behavior. A SET is electrically masked when the pulse resulting from a particle hit is attenuated due to the electrical properties of

the gates on its propagation path so that the resulting pulse is of insufficient magnitude to be reliably latched. Last but not least, the third factor which contributes to the elimination of such disturbances in the circuits is ***timing masking*** and occurs when a TF arrives at the input of a FF outside of the latching window where the memory element capture the input value.

III. METHODOLOGY OF SER ESTIMATION

In this section, a layout-based SER estimation in the presence of MTFs in combinational logic is presented. Firstly, we describe the method utilized to identify the affected areas due to a particle strike, and then, we elaborate the structure of the respective algorithm and a grid analysis along with the way that the masking effects are incorporated into the proposed tool in order to obtain a preview of circuits' vulnerability to such type of errors.

A. Placement-aware Analysis of SEMTs

When a high-energy particle strikes a sensitive region of a cell, a voltage glitch, that is a SET, may be produced at the output. On the contrary, SEMTs occur when a particle does not affect only a single point of the chip but an area, which should be defined properly for an accurate particle strike simulation [15], [31]. Thus, a number of transistors may be affected resulting in a flip on the logic state of the corresponding gates' output. The affected area is mostly a function of particle energy. For this reason, the corresponding data can be applied even on different technologies [26]. The higher the amount of energy is, the wider the area of the circuit that is affected by the strike. This surface is depicted with oval shapes, according to the average affected area for each particle's energy, as shows Table I [23].

TABLE I. AVERAGE AFFECTED AREA

Particle Energy (MeV)	Average Affected Area (μm^2)
22	1.178
47	1.902
95	2.903
144	4.613

As regards the implementation of this novel SEMTs approach, particle hits are injected on random points into the die area of each circuit. The respective oval shapes indicate which transistors, and hence which gates, are affected by each particle strike. The radius of the oval shape corresponds to the range that a particle hit affects, as shown in Fig. 2. If a sensitive transistor is located within the range of the strike, a SET is created on the corresponding gate's output. Furthermore, Fig. 2 shows the result, with respect to the affected area, of two particle strikes with different energies [25], [29], [30].

The identification of the physically adjacent cells of each circuit is a considerable step for the SEMT analysis. There are approaches which rely only on logic-level netlist, neglecting cells' adjacency and considering a gate and its fan-ins, a gate and its fan-outs, fan-ins of a gate and fan-outs of a gate as adjacent nodes for multiple transients' error sites [27], [28]. In this context, when a particle strikes a random area of a circuit and affects a gate, its fan-out may lead to a gate which does not belong to the same error sites, according to the actual layout. Thus, considering only logic-level netlists during the analysis leads to inaccurate estimation of SER, since, with this method, a restricted number of cells are physically adjacent.

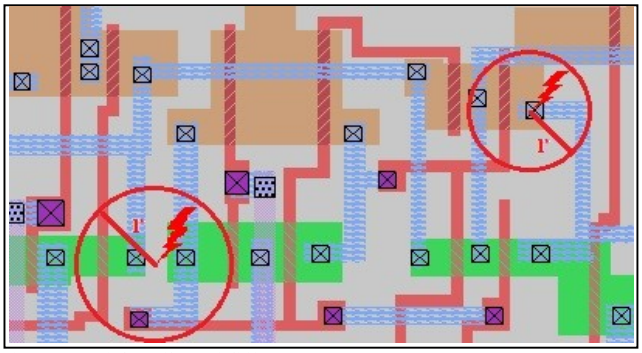


Fig. 2. Particle strikes of different energy

For this purpose, in this work, the *DEF (Design Exchange Format)* files - for the corresponding ISCAS' 89 benchmark circuits - have been utilized [29], [30]. These files describe the position and placement direction of each logic cell in the layout. Along with the GDSII files we are able to define the transistors' position of each gate on the die area. The determination of the gates' sensitive zones is mandatory, since we regard as affected cells only those whose inactive transistors are located within the oval shapes. To sum up, our methodology is based on the gates' placement locations of each circuit, the aforementioned methodology for the identification of the sensitive zones of each affected cell, and the masking phenomena modeling in order to estimate accurately SER.

B. Proposed Algorithm

Monte-Carlo simulation is the basis of the proposed methodology for the evaluation of SER [5], [10]. The execution of *10,000* simulations with different input vectors seems to be adequate, since, as this number increases the divergence in the result is negligible. Although this method is time consuming, is preferable from other probabilistic methods, as it provides secure estimation [15]. Also, a couple of acceleration techniques succeeded in reducing the execution time especially for the large-scale benchmarks.

The implemented tool is based on a simple zero-delay gate-level simulator. Particularly, logical effort has been utilized to determine the gates' delay, since it is considered a straightforward delay estimation technique. A key point for the proposed implementation is the treatment of the MTFs propagation concerning the three masking effects. In particular, each pulse, originated from a single particle strike, that appears at the output of the affected cells propagate throughout the circuit along with its own logical, electrical and timing masking information. In order to examine each error separately, and determine those that will be captured by the memory elements, three tables for each circuit node have been used, one for each masking effect, while

their size changes dynamically and depends on the number of MTFs generated from a particle strike.

Regarding the modeling of logical masking, the corresponding table holds the logic state of each node as well as the new state after the faults generation. Thus, we determine which faults propagate through the circuit to the inputs of the FFs and which are logically masked. For the timing masking, it is necessary to compute the overall time for each fault, that is, the time it takes to reach the FF from the moment of the SEMTs incident. A glitch is captured by a FF only if it arrives at the data input during the latching window. Finally, electrical masking is modeled along with the aforementioned mechanisms. The generated glitches have initially the same width, while the main factor that affects their value is the gate delay. As regards the reconvergent transient pulses, we handle the case of a fault reconverging at a gate, following different paths, at the same time. Particularly, when two or more pulses of the same transient fault reconverge at a cell having the same direction, the output pulse is the sum of the input pulses. On the other hand, as for the overlapping pulses with opposite direction, the resulting pulse at the output of the gate depends on its type and controlling value. Therefore, during the simulation, this information, for each pulse, is updated while the signal passes through the subsequent cells until the inputs of the memory elements. Taking into account the final values, if at least one of these pulses gets latched by any of the flip-flops then a soft error is counted. Masking effects are used to estimate the total latching probability for each simulation, comparing initially the input logic state of each FF with the pointer estimated for the logical masking and then all together. As a result, the overall SER is estimated considering the latching probabilities of each simulation.

C. *Grid Analysis*

The purpose of a well-designed and accurate SER estimation tool is to provide to VLSI designers an overview of the vulnerability of a circuit so as, by making tradeoffs between power, performance and reliability, they will be able to construct error-resistant chips [25], [30].

In this context, the layout of each circuit has been equally divided into a hundred smaller parts, called so on *grids*, and are considered as small sub-circuits. Particularly, a number of particle hits are injected on each grid causing a different number of errors since each sub-circuit includes its own set of logic cells placed in this area. Afterwards, the aforementioned methodology is applied for each grid in order to obtain the overall SER of the circuits. This process facilitates the identification of susceptible sites as well as the extraction of reliable outcomes by exciting the entire circuit. Fig. 3 shows the SER of some grids of S35932 benchmark accounting for the number of gates and FFs.

We conclude from this graph that the grids which contain a large number of gates and FFs are more probable to have a greater overall number of errors occurred from a particular number of particle hits. However, something that should be underlined is that the existence of many faults in some blocks does not mean that the respective SER is greater than others with less. Particularly, the estimation of SER depends on the type of gates that are located on each grid and how the masking effects influence this process. For example, although sub-circuits 53 and 100, as shown in Fig. 3, have several gates and FFs, their SER is approximately zero. Thus, it could be deduced that these factors may affect more drastically these grids or, maybe, the energy of the particle strikes on these parts of the circuit was not intense enough to cause many errors.

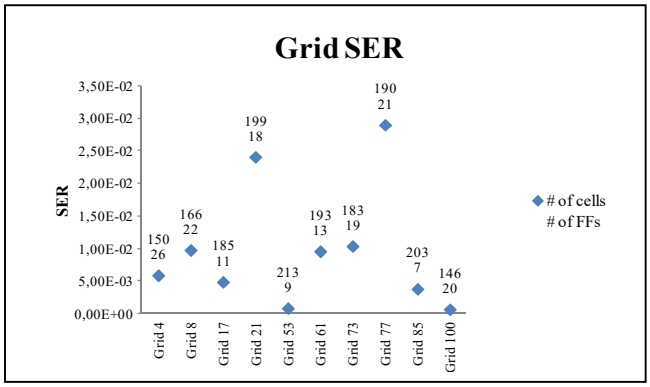


Fig. 3. GRIDS' SER of S35932

Furthermore, we infer from these results that sensitive grids should be regarded those that are close to flip-flops, since generating pulses are more possible to reach at the memory elements. We consider as *Gate group1* the number of the gates of each grid that lead to FFs that belong to the same grid with them. Nevertheless, some gates, which belong in *Gate group2*, may lead to flip-flops which are located to other grids. This could explain the fact that different sub-circuits, which have similar number of gates and FFs, have a significant difference in SER. For instance, in Fig. 3 and Fig. 4, the SER and the percentage of gates of-group1 for grid 21 are both greater compared to the respective for grid 17. For the grid 100, as mentioned previously, the calculation of SER may be affected by the masking factors, since, as shown in Fig. 4, the fact that the majority of its gates lead to FFs of the same grid does not explain the almost zero value of SER. On the other hand, as regards grid 53, the principal cause of such a low SER seems to be the connection between its gates and the memory elements, since only 9 gates drive FFs of the same grid.

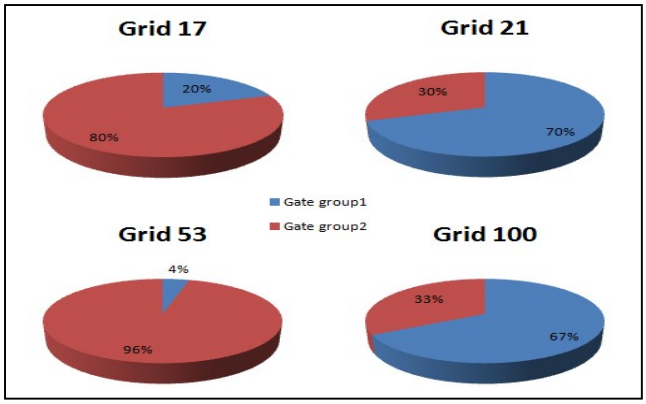


Fig. 4. Gates' connectivity with FFs of S35932

IV. RESULTS

In this section, we will present the results of the experiments and for this purpose, as already mentioned, *ISCAS'85 and ISCAS'89* benchmark circuits have been used. Furthermore, the proposed tool was run on an Intel Core i3-4005U @1.7GHz machine with 4 GB RAM.

Several techniques have been used to speed up the simulation. One of them is to hold the logic state of each node on an *unsigned int* variable where each position of the 32-bit number corresponds to one separate simulation. In this way, we take advantage of all possible combinations of primary inputs. Therefore, at the end of a single iteration, 32 different primary inputs have been used and, thus, 32 different simulations have been completed.

As discussed in the previous sections the sensitive zones of a transistor and the energy of a particle strike are determinant factors for the calculation of SER with regard to the affected areas of a circuit. However, another key factor is the modeling of the pulse width. According to [32] and [33], the SET pulse width is a function of operating temperature. Particularly, the actual measurements show that the width increases with the temperature [32]. Integrating these data into our tool, Fig. 5 shows the estimated SER for three different temperatures and for a particle energy of 47 MeV $\cdot$ cm^2/mg. The results indicate that at the temperature of 100°C, SER is greater in comparison with the other cases. That seems absolutely reasonable since the attenuation of the generated pulses is not that intense so as to be completely eliminated and, thus, it is more likely to be latched by memory elements.

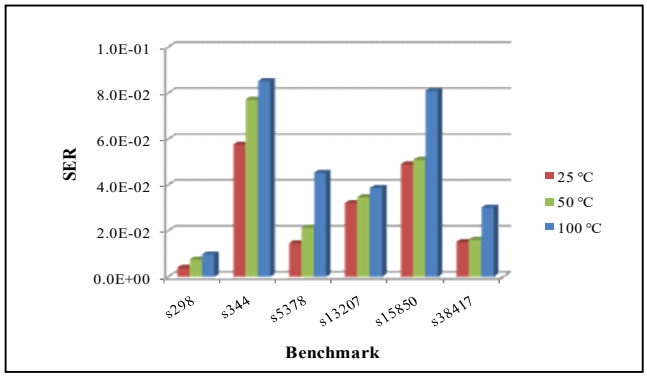


Fig. 5. Estimation of SER as a function of temperature

It is worth mentioning that the current technology is not the only factor that impacts on the configuration of SET pulse width, since it is also a function of the circuit topology through which the SET propagates [34]. For this reason our approach make use of the pulse widths for the particular temperatures obtained from [32], even thought the measurements have been made for the 65-nm process while we utilize a 45-nm technology. Furthermore, according to [32], in PMOS transistors the parasitic bipolar effect is worse than in NMOS transistors and, thus, the generated pulses are larger when a particle strikes an inactive PMOS transistor. This means that the overall SER is expected to be higher when the hits on the PMOS transistors are significantly more than on the NMOS. Particularly, the average SET pulse width for the sensitive PMOS transistors is regarded to be 128 ps at 25°C, 160 ps at 50°C, and 202 ps at 100°C, while the width for the sensitive NMOS transistors is considered to be 118 ps, 140 ps, and 158 ps, respectively.

Table II presents the evaluation of SER obtained from the proposed tool for some benchmark circuits, as well as the corresponding execution time. The range of the affected area due to a particle strike is determined by the energy of the particle, while the SET pulse width depends on the transistor's parameters and the operating temperature. Moreover something should be highlighted is that the selection of energy of particle hit is occurred randomly by the simulator and the temperature remains stable at 25°C.

TABLE II. SER AND EXECUTION TIME OF BENCHMARK CIRCUITS

Benchmark	# of nodes	# of gates	# of DFFs	SER	Exec. time
S400	192	188	21	0.012485	42 sec.
S1423	750	733	74	0.017326	~ 2 min.
S9234	5870	5834	211	0.018341	~ 17 min.
S15850	10425	10348	534	0.049041	~ 35 min.
S35932	17837	17802	1728	0.011752	~ 58 min.

To be able to verify the obtained results from our implementation, a SPICE simulator is used for the sequential circuits S27, S298 and S400 (Fig. 6) [13], [17]. SPICE simulation is generally a time consuming process especially for larger circuits. For this reason, for these circuits, only one hundred simulations are carried out injecting current pulses to random nodes of each SPICE netlist as described in subsection III.A and on different time moments. Thus, our tool is regarded accurate in comparison with SPICE simulations since a number of *10,000* simulations provide a reliable estimation of SER.

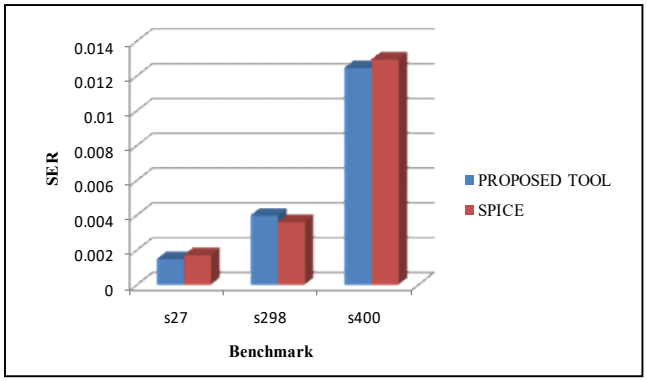


Fig. 6. SER verification

V. CONCLUSION

In this work, a Monte-Carlo-based approach for an accurate estimation of the vulnerability of ICs to radiation-induced faults is proposed, taking into consideration MTFs. In this direction, the placement details of each circuit are utilized for the identification of the multiple transients. The simulation results provide to VLSI designers information

about the sensitivity of particular parts of a chip. This could facilitate the placement process and, consequently, the development of error-resistant circuits.

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